HW#8 디지털 회로 설계 및 언어 월수 9:00~10:15 2015104027 박정진

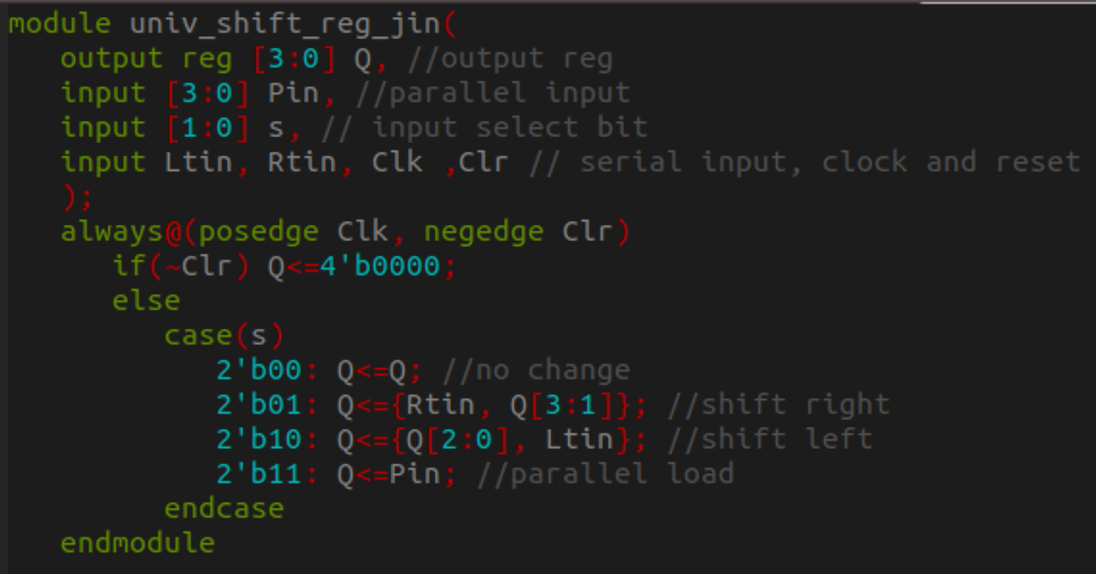
1. function table

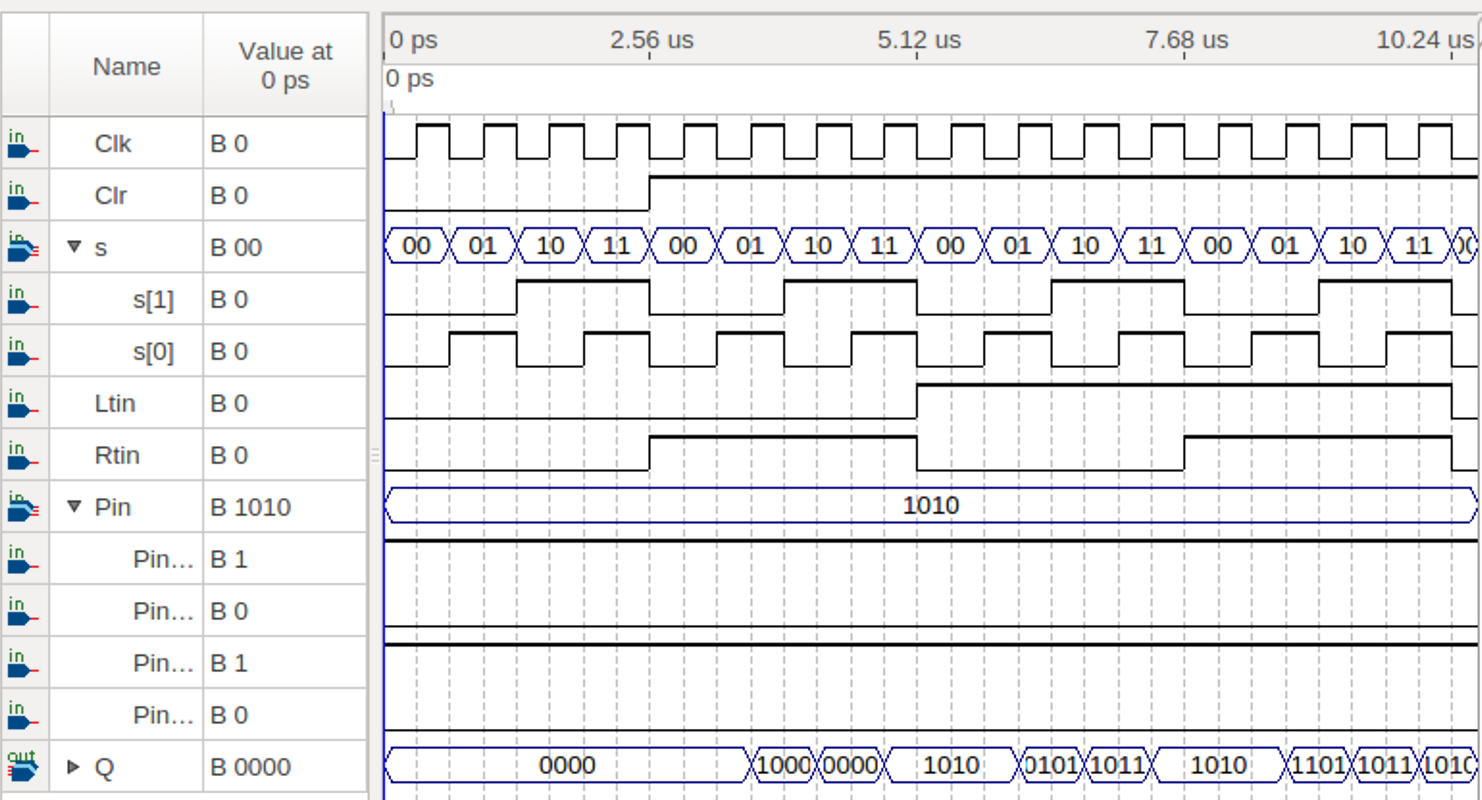
Positive edge triggered Universal shift register function table with asynchronous reset and synchronous parallel load with control bit

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Clk | Clrn | Control bit | | Function |
| s[1] | s[0] |
| x | 0 | 0 | 0 | No change |
|  | 1 | 0 | 1 | Shift Right |
|  | 1 | 1 | 0 | Shift Left |
|  | 1 | 1 | 1 | Parallel Load |

2. Verilog code and simulation using vwf

->on next page





|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Clk | Clr | s[1:0] | Ltin | Rtin | Pin | Q | Function |
| t=2.56us | x | 0 | x | x | x | x | 0000 | clear |
| t=2.88us |  | 1 | 00 | 0 | 1 | 1010 | 0000 | No change |
| t=3.52us |  | 1 | 01 | 0 | 1 | 1010 | 1000 | Shift right(Rtin=1) |
| t=4.16us |  | 1 | 10 | 0 | 1 | 1010 | 0000 | Shift left(Ltin=0) |
| t=4.8us |  | 1 | 11 | 0 | 1 | 1010 | 1010 | Parallel Load |
| t=5.44us |  | 1 | 00 | 1 | 0 | 1010 | 1010 | No change |
| t=6.08us |  | 1 | 01 | 1 | 0 | 1010 | 0101 | Shift right(Rtin=0) |
| t=6.72us |  | 1 | 10 | 1 | 0 | 1010 | 1011 | Shift left(Ltin=1) |
| t=7.36us |  | 1 | 11 | 1 | 0 | 1010 | 1010 | Parallel Load |
| t=8us |  | 1 | 00 | 1 | 1 | 1010 | 1010 | No change |
| t=8.64us |  | 1 | 01 | 1 | 1 | 1010 | 1101 | Shift right(Rtin=1) |
| t=9.28us |  | 1 | 10 | 1 | 1 | 1010 | 1011 | Shift left(Ltin=1) |
| t=9.92us |  | 1 | 11 | 1 | 1 | 1010 | 1010 | Parallel Load |